VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME

Abstract of the Disclosure

A vertical gain memory cell including an n-channel metal-oxide semiconductor field-effect transistor (MOSFET) and p-channel junction field-effect transistor (JFET) transistors formed in a vertical pillar of semiconductor material is provided. The body portion of the p-channel transistor is coupled to a second source/drain region of the MOSFET which serves as the gate for the JFET. The second source/drain region of the MOSFET is additionally coupled to a charge storage node. Together the second source/drain region and charge storage node provide a bias to the body of the JFET that varies as a function of the data stored by the memory cell. A non destructive read operation is achieved. The stored charge is sensed indirectly in that the stored charge modulates the conductivity of the JFET so that the JFET has a first turn-on threshold for a stored logic "1" condition and a second turn-on threshold for a stored logic "0" condition. The charge storage node is a plate capacitor which surrounds the second source/drain region of the MOSFET. The vertical gain cell is fabricated so that the write word line, read bit line, read word line and capacitor are buried beneath the silicon surface. As a result the cell can be fabricated in an area as small as four (4) lithographic feature squares.